IN THE SPECIFICATION

Please amend the paragraph at page 5, lines 1-4 as follows:

Embodiments of the invention may include detection circuitry ~~1~~ for monitoring one or more switches. The exemplary embodiment of the present invention described hereinbelow is a circuit for monitoring the state of two switches. The circuitry for monitoring one switch may be the same as the circuitry for monitoring the other switch.

Please amend the paragraph at page 5, lines 5-9 as follows:

The detection circuitry ~~1~~ may include circuitry for selecting one of the detection configurations. When a configuration is selected, circuitry dedicated to the unselected configurations may be disabled and decoupled from the switch. A configuration register (not shown), for example, may store data which is used to perform the selection. In this way, the configuration may be set in a volatile manner.

Please amend the paragraph at page 5, lines 10-15 as follows:

Figures 1A and 1B illustrate a block diagram of the detection circuitry ~~1~~ associated with two switches S1 and S2. Switches S1 and S2 may be of virtually any switch type, and are depicted in symbolic form for reasons of simplicity. Each switch S1 and S2 has a conduction terminal coupled to detection circuitry ~~1~~. A conduction terminal of switch S1 is coupled to node TP1 of detection circuitry ~~1~~, and a conduction terminal of switch S2 is coupled to node TP2. The configuration register (not shown) may provide many of the input signals to detection circuitry ~~1~~.

Please amend the paragraph at page 5, lines 16-19 as follows:

Normally open circuits 3 monitor the two switches S1 and S2 when detection circuitry ~~1~~ is configured in the normally-open tamper configuration. In particular, each of the blocks 3 is used to monitor a distinct switch S1 or S2 when detection circuitry ~~1~~ is configured in either the normally-open-tamper-to-high configuration or the normally-open-tamper-to-low configuration.

Please amend the paragraph at page 5, line 20 to page 6, line 6 as follows:

Detection circuitry ~~1~~ further includes normally closed circuits 5, each of which is to adapted to monitor a distinct switch S1 or S2 when detection circuitry ~~1~~ is configured in one of the normally-closed tamper configurations. Normally closed circuits 5, when enabled, are capable of monitoring switches S1 and S2 when detection circuitry ~~1~~ is configured in either the normally-closed-tamper-to-low or normally-closed-tamper-to-high configurations. Output circuits 7 receive the outputs of each normally open circuit 3 and normally closed circuit 5 and generates a pair of output signals TB1 and TB2 having values representative of switch S1 and S2, respectively, changing state.

Please amend the paragraph at page 9, line 17 to page 10, line 3 as follows:

Circuitry 110 may also include a circuit 45, control circuit (TAMPERSEL) 46 and flip flop circuit 11 connected to each other much as such circuits are connected to each other in circuitry 100. In addition, circuitry 110 may include logic NOR gate 80 coupled between circuitry 45 and flip flop circuit 11 of circuitry 110. An n-channel transistor 48 may be coupled between signal TP and the low voltage reference. The control

terminal of transistor 48 is coupled to the output of circuit 45 of circuitry 110. Transistor 48 is sized to relatively weakly pull signal TP (and thus the conduction terminal of a switch S1 or S2) towards the low voltage reference when activated (i.e., when the switch remains normally open).

Please amend the paragraph at page 10, lines 4-14 as follows:

As stated above, circuit 120 serves to enable one or less circuits 100 and 110, based upon the desired configuration for detection circuitry ~~1~~. Input signal Control1 controls whether one of circuit 100 and 110 will be enabled to monitor the corresponding switch. Signal Control1 may be in a first (logic high, in this exemplary embodiment) state when detection circuitry ~~1~~ is configured in a normally open configuration, and in a second (logic low) state when detection circuitry ~~1~~ is configured in a normally closed state. Control signal Control2 selects the circuit 100 or 110 that is enabled for monitoring the corresponding switch. When signal Control2 is in a first (logic low) state, circuit 100 is enabled to monitor the corresponding switch and detection circuitry ~~1~~ is thus configured in the normally-open-tamper-to-low state. Conversely, when signal Control2 is in a second (logic high) state, circuit 110 is enabled to monitor the corresponding switch and detection circuitry ~~1~~ is thus configured in the normally-open-tamper-to-high state.

Please amend the paragraph at page 12, lines 3-8 as follows:

Figures 3A and 3B are a schematic diagram for each of the normally closed circuits 5 appearing in Figures 1A and 1B. Each normally closed circuit 5 may include a string of series-connected resistors and a plurality of pass gate transistors coupled thereto that may be controlled (i.e., activated or deactivated) for configuring detection

circuitry 4 to be one of the normally-closed-tamper-to-high and normally-closed-tamper-to-low configurations. The normally closed circuit 5 receives input signal TP which is coupled to a conduction terminal of the switch being monitored.

Please amend the paragraph at page 12, lines 9-17 as follows:

Figure 4 illustrates a simplified schematic of the resistor-pass gate transistor circuitry normally closed circuit 5 of Figures 3A and 3B for configuring the detection circuitry 4 to be in one of the normally-closed-tamper-to-high and normally-closed-tamper-to-low configurations. The simplified schematic of Figure 4 shows a resistor R, which may be formed from a plurality of series-connected resistors; transistor 400 coupled between the high reference voltage Vcc and resistor R; transistor 402 coupled between the low reference voltage Vss and resistor R; transistor 403 coupled between input signal TP and the node coupling transistor 400 to resistor R; and transistor 404 coupled between input signal TP and the node coupling transistor 402 to resistor R. The control terminal of each transistor 400-402 is coupled to control signals.

Please amend the paragraph at page 12, line 18 to page 13, line 5 as follows:

When the detection circuitry 4 is configured in the normally-closed-tamper-to-high configuration, transistors 400 and 404 are activated and transistors 402 and 403 are deactivated. This results in resistor R being coupled to the switch being monitored as a pull-up resistor. When the switch is normally closed, input signal TP is pulled to a voltage corresponding to a logic low state due to the drive strength of the switch being greater than that of the pull-up transistor. Then, when the switch is opened, resistor R pulls input signal TP to a voltage representing a logic

high state. Input signal TP being in the logic high state causes circuitry in Figures 1A and 1B to drive a corresponding output signal TB1 or TB2 to a logic state to initiate additional tasks.

Please amend the paragraph at page 15, lines 3-8 as follows:

An operation of detection circuitry ~~1~~ will be described with reference to Figure 7. Initially, detection circuitry ~~1~~ is configured into one of the four possible configuration states discussed above. Configuring detection circuitry ~~1~~ into a selected state disables the circuitry associated with the three unselected states. The step of configuring may be performed by loading the configuration register, whose outputs control circuitry in normally open circuits 3 and normally closed circuits 5.

Please amend the paragraph at page 15, lines 9-18 as follows:

In the event detection circuitry ~~1~~ is configured in the normally-closed-tamper-to-high configuration, normally open circuits 3 are disabled from monitoring the switches S1 and S2 and thus do not affect the outputs TB1 and TB2. Transistors 400 and 404 are activated and transistors 402 and 403 are deactivated, which results in resistor R of each normally open circuit 5 acting as a pull-up resistor. When a switch S1 or S2 changes to the open state, such as in response to the occurrence of a tamper condition, the corresponding normally closed circuit 5 detects signal TP being pulled to the logic high state resistor R. Circuitry in normally closed circuit 5 detects node TP being pulled to the logic high state, and drives output TB to a value indicative of the detection. Output circuits 7 responsively drive the output TB1 to a value indicative of the detection of the switch being opened.

Please amend the paragraph at page 15, line 19 to page 16, line 4 as follows:

In the event detection circuitry 4 is configured in the normally-closed-tamper-to-low state, a similar set of steps are performed as described above. However, transistors 402 and 403 are activated and transistors 404 are deactivated, resulting in the resistor R forming a pull-down resistor. Normally closed circuit 5 associated with a switch that opens detects node TP being pulled to a logic low value by resistor R, and output TB1 or TB2 is driven to a state indicative of the detection.

Please amend the paragraph at page 16, lines 4-12 as follows:

In the event detection circuitry 4 is configured in the normally-open-tamper-to-high state, normally closed circuits 3 are disabled and do not perform the above-described detecting. Transistor 47 (Figures 2A and 2B) is activated and transistor 48 is deactivated by circuit 120 and signals Control1 and Control2. Activated transistor 47 pulls node TP (and hence the conduction terminal coupled thereto) to a logic high value. When a switch closes, such as due to the occurrence of a tamper event, node TP is pulled to a logic low value. This results in transistor 47 being deactivated and flip flop circuit 11 of circuit 100 clocking a logic high data value, which causes output TB to be in a logic high state, which thereupon causes the output of output circuits 7 to indicate the detection of the switch being closed.

Please amend the paragraph at page 16, lines 13-21 as follows:

In the event detection circuitry 4 is configured in the normally-open-tamper-to-low state, normally closed circuits 3 are disabled and do not perform the above-described detecting. Transistor 48 (Figures 2A and

2B) is activated and transistor 47 is deactivated by circuit 120 and signals Control1 and Control2. Activated transistor 48 pulls node TP (and hence the conduction terminal coupled thereto) to a logic low value. When a switch closes, such as due to the occurrence of a tamper event, node TP is pulled to a logic high value. This results in transistor 48 being deactivated and flip flop circuit 11 of circuit 110 clocking a logic high data value, which causes output TB to be in a logic high state, which thereupon causes the output of output circuits 7 to indicate the detection of the switch being closed.